each of the nonvolatile semiconductor memory devices comprising:

a word gate formed on a semiconductor layer with a first gate insulating layer therebetween;

an impurity diffusion layer which forms either a source region or a drain region;

a first control gate formed along a first side of the word gate, the first control gate being disposed on the semiconductor layer with a second gate insulating layer therebetween, and also on the word gate with a side insulating layer therebetween;

a second control gate formed along a second side of the word gate, the second control gate being disposed on the semiconductor layer with another second gate insulating layer therebetween, and also on the word gate with another side insulating layer therebetween;

the first and second control gates extend in a first direction; and

an end of the first control gate and an end of the second control gate that are adjacent to each other in a second direction which intersects the first direction, being connected to a common contact section.--

--14. The semiconductor integrated circuit device of claim 13, wherein the first and second control gates are formed in the shape of sidewalls along either side of the word gate.--

--15. The semiconductor integrated circuit device of claim 13, wherein the common contact section includes an insulating layer formed on the semiconductor layer, the insulating layer formed of a laminate comprising a first silicon oxide layer, a silicon nitride layer, and a second silicon oxide layer.--

--16. The semiconductor integrated circuit device of claim 13, wherein the common contact sections are staggered relative to each other.--

--17. A semiconductor integrated circuit device having a memory cell array in which nonvolatile semiconductor memory devices are arranged in a matrix with a plurality of rows and columns,

wherein each of the nonvolatile semiconductor memory devices comprises:

a word gate formed on a semiconductor layer with a first gate insulating layer therebetween;

an impurity diffusion layer that forms either a source region or a drain region; and

first and second control gates formed along either side of the word gate in the shape of sidewalls, wherein:

the first control gate being disposed on the semiconductor layer with a second gate insulating layer therebetween, and also on the word gate with a side insulating layer therebetween;

the second control gate being disposed on the semiconductor layer with another second gate insulating layer therebetween, and also on the word gate with another side insulating layer therebetween;

the first and second control gates extend in a first direction; and

an end of the first control gate and an end of the second control gate of a pair of gates adjacent to each other in a second direction which intersects the first direction, being connected to a common contact section that is disposed in a staggered arrangement relative an adjacent common contact section.--

--18. A semiconductor integrated circuit device having a memory cell array in which nonvolatile semiconductor memory devices are arranged in a matrix with a plurality of rows and columns,

wherein each of the nonvolatile semiconductor memory devices comprises:

a word gate formed on a semiconductor layer with a first gate insulating layer therebetween;

an impurity diffusion layer which forms either a source region or a drain region; and

first and second control gates in the shape of sidewalls formed along either side of the word gate, wherein:

the first control gate is disposed on the semiconductor layer with a second gate insulating layer therebetween, and also on the word gate with a side insulating layer therebetween;

the second control gate is disposed on the semiconductor layer with another second gate insulating layer therebetween, and also on the word gate with another side insulating layer therebetween;

the first and second control gates extend in a first direction; and

a pair of the first and second control gates, adjacent in a second direction which intersects the first direction, is connected to a common contact section that is disposed in a staggered arrangement relative an adjacent common contact section.--

--19. The semiconductor integrated circuit device of claim 18, wherein the common contact section includes an insulating layer formed on the semiconductor layer, the insulating layer formed of a laminate comprising a first silicon oxide layer, a silicon nitride layer, and a second silicon oxide layer.--

REMARKS

Claims 1-19 are pending. By this Amendment, claim 7 is amended and new claims 13-19 are added. Reconsideration based on the above amendments and following remarks is respectfully requested.

The attached Appendix includes a marked-up copy of the rewritten claim (37 C.F.R. §1.121(c)(1)(ii)).